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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,968	01/29/2004	Dominique Mangelinck	ASTAP2004-01	1967

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HORIZON IP PTE LTD
8 KALLANG SECTOR, EAST WING
7TH FLOOR
SINGAPORE 349282, 349282
SINGAPORE

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,968	MANGELINCK ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36 and 38-41* is/are rejected.

7)☒ Claim(s) *37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 37 objected to because of the following informalities: The claim is identical to claim 29. Appropriate correction is required.

Inclaim 29, line 5, following the letter consumption, "or" should be changed to "of". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 5, 8, 10 – 12, 15, 16, 18 – 20, 22, 23, 25, 26 – 28, 30 – 36 and 38 – 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Moslehi, US 5,397,909.

Regarding claim 1, Moslehi teaches a method of fabricating a gate electrode for a semiconductor comprising the steps of:

- providing a substrate 38 (Fig. 17);
- providing on the substrate a layer of a first material, 92, 94, 96 of thickness t_p , the first material being selected from the group consisting of Si, $Si_{1-x} - Ge_x$ alloy, Ge and mixtures thereof (column 15, lines 39 – 46) and a layer of metal 97 of thickness t (Fig. 18); and annealing the layers, such that substantially all of the first material and the metal are consumed during reaction with one another (Fig. 19) in between column 18, line 51 and column 19, line 40.

Regarding claims 2 and 25, Moslehi teaches the metal Ti in column 6, line 33.

Regarding claim 3, Moslehi teaches the first material layer is applied to the substrate and the metal layer is provided on the first material layer with reference to Fig. 18.

Regarding claims 4 and 5, Moslehi teaches the thicknesses t_p and t_m are related by a predetermined ratio of t_m / t_p and the ratio is determined by the first material and the metal since sometimes the reaction does not consume all of the metal and the materials are chosen for their work function.

Regarding claim 8, Moslehi teaches forming source/drain contacts 98 simultaneously with the gate electrode with reference to Fig. 18.

Regarding claim 10, Moslehi teaches the gate electrode for a semiconductor device comprising a substrate and a gate layer thereon formed by the annealing of a first material with a metal, substantially all of the first material and the metal having been consumed during reaction with one another, the resultant layer comprising the gate electrode with reference to Figs 17 and 18 as was described earlier in rejecting claim 1.

Regarding claims 11 and 12, Moslehi teaches these limitations as was described earlier in rejecting claims 1 and 2.

Regarding claim 15, Moslehi teaches the gate electrode is incorporated in a CMOS semiconductor device in column 2, lines 36 – 40.

Regarding claims 16, 18 and 19, Moslehi teaches all limitations of the claim as described earlier in rejecting claim 1. The first layer material such as Si – Ge alloys

inherently have the work functions close to the mid – gap energy of semiconductor material such as silicon.

Regarding claims 20, 23, 27, 28, 30, 32, 33, 35, 38 and 40, Moslehi teaches Annealing or RTA in column 19, lines 18 – 39.

Regarding claims 22, 26, 31, 34 and 39, Moslehi teaches metal layer forms silicide over the diffusion regions with reference to Fig. 19.

Regarding claim 33, Moslehi teaches etching remaining portion of unreacted metal layer above the gate electrode after processing the metal layer in column 19, lines 40 – 42.

4. Claim 41 is rejected under 35 U.S.C. 102(b) as being anticipated by Bulucea, US 5,952,701.

Bulucea teaches an integrated circuit comprising a transistor having a gate electrode and first and second diffusion regions wherein the gate electrode is formed from an amorphous polycrystalline first layer comprising a material having a work function close to the mid – gap of silicon band gap, the material reduces problems associated with inversion and agglomeration associated with formation of the transistor with reference to Fig. 16 and associated descriptions under columns 38 and 39. The reduction of problems associated with inversion and agglomeration associated with formation of the transistor is inherent in the materials and the process. This is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this

issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 9, 13, 17, 21, 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi, US 5,397,909.

Regarding claims 9, 13, 21 and 24, Moslehi teaches that complete consumption of the metal for the silicide is not necessary but fails to teach as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the thickness of the twp materials and the reaction time and temperature during the during the silicide formation through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) in terms of of desired work function.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

Regarding claim 17, Molshehi fails to teach patterning the first layer comprises forming gate electrodes of at least a first PMOS transistor and a first NMOS transistor to

form a CMOS integrated circuit and the material of the first layer comprises silicon, germanium, alloys or a combination thereof, including Si_{1-x} Ge_x.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention that since Molsehi teaches the formation of the gate for a MOS transistor it can be applied to forming CMOS integrated circuitry since CMOS transistors cosists of two types of MOS transistors.

Regarding claim 29, Moslehi teaches the thicknesses t_p of the first layer and thickness t_m of the metal layer but fails to teach having a minimum ratio of t_m /t_p and the minimum ratio results in consumption of substantially of both materials.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention that a minimum ratio will mean a smaller thickness of the metal compared to the silicon and therefore during annealing most of the metal layer will react to form the silicide layer.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi, US 5,397,909 in view of Theng, US 5,705,417.

Molshehi fails to teach the annealing temperature.

Theng teaches the annealing temperature of 300 – 900 ^{O}C for the benefit of reacting to form the silicide in column 5, lines 4 – 7.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Moslehi to carry the annealing at a temperature of 300 – 900 ^{O}C for the benefit of reacting to form the silicide as taught by Theng in column 5, lines 4 – 7.

10. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi, US 5,397,909 in view of Nguyen, US 6,084,279.

Molshehi fails to teach the step of depositing a further layer of metal on the gate electrode to increase gate thickness.

Nguyen teaches that a metal layer such as 66 (Fig. 8) can be added to the gate electrode in column 5, lines 35 – 46 for the benefit of matching the work function of the gate to that of the substrate in column 1, lines 44 – 45 which in turn also increases the thickness of the gate.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Molshehi and deposit a further layer of metal on the gate electrode to increase gate thickness for the benefit of matching the work function of the gate to that of the substrate as taught by Nguyen in column 1, lines 44 – 45.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Asok Kumar Sarkar

Asok K. Sarkar
August 15, 2006

Primary Examiner